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Wire Shorting Defect Mitigation on Substrate LGA Device through Wirebond Capillary Adjustment

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Authors' contributions

This work was carried out in collaboration among all authors. All authors read and approved the final manuscript.

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ABSTRACT

Semiconductor packaging technologies are getting more challenging with regards to assembly manufacturing due to several factors such as complex package layout, process and machine capability, and materials compatibility. This paper discusses the wirebonding process difficulty and the solution to mitigate the wire-to-wire shorting defect on a substrate land grid array (LGA) device that causes low yield on engineering trials. Using a high-speed camera equipment, the actual process was monitored. It was then noticed that the cause of wire-to-wire shorting issue was a capillary hitting on previous wire. Ultimately, with the new capillary design and process optimization, wire-to-wire shorting defect was successfully mitigated.

Keywords: Capillary; LGA; substrate; wirebonding; wire-to-wire shorting.

1. INTRODUCTION

Critical wirebonding layout in substrate land grid array (LGA) device is a big challenge to realize in actual wirebonding process. Note that with new and continuous technology trends and state-of-the-art platforms, these manufacturing challenges are

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inevitable [1-4]. The device in focus is applying reverse bonding on its wirebonding process to provide interconnection between the topmost die and the lead fingers on the substrate. However, wire-to-wire shorting defect as shown in Fig. 1 was encountered during the engineering trials, and this in turn affected the yield performance. This paper presents the solution to address the wirebonding issue.

A complete assembly process flow for the device in focus starting from pre-assembly to singulation is given in Fig. 2. Important to note that assembly manufacturing processes vary with the technology and the product [5-8].

Wire-to-wire shorting was the top assembly reject in wirebonding process and this was observed during lot processing of the device. During wirebond looping process, parameter optimization is normally done but the parameter is not enough to solve the issue encountered for the device.

2. METHODS, RESULTS AND DISCUSSION

Wirebond parameter optimization was comprehensive done particularly on wirebond looping, but still wire-to-wire shorting appeared. With this, the actual process was closely monitored. It was then noticed with the aid of a high-speed camera equipment that the cause of wire-to-wire shorting issue is the capillary bottle neck hitting the adjacent wire. The dimension of the capillary was checked and discovered that its 14 mils in height.

The capillary was redesigned and adjusted with higher bottle neck with 20 mils in height, taking into consideration the wire size and the clearance between adjacent wires. With the new capillary design used for validation, no more wire-to-wire shorting and capillary hitting occurrence were observed. The implementation of the redesigned capillary significantly contributed to the improvement in the wirebond process yield performance as shared in Fig. 3. Note that actual values are intentionally not shown due to confidentiality. Lastly, Fig. 4 shows

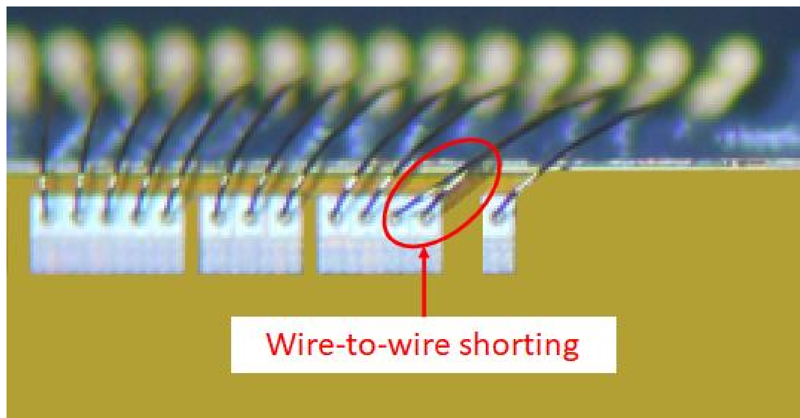

Fig. 1. Wire-to-wire shorting defect

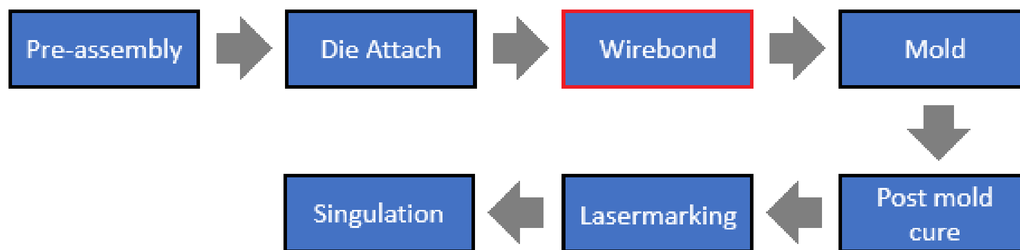

Fig. 2. Assembly process flow

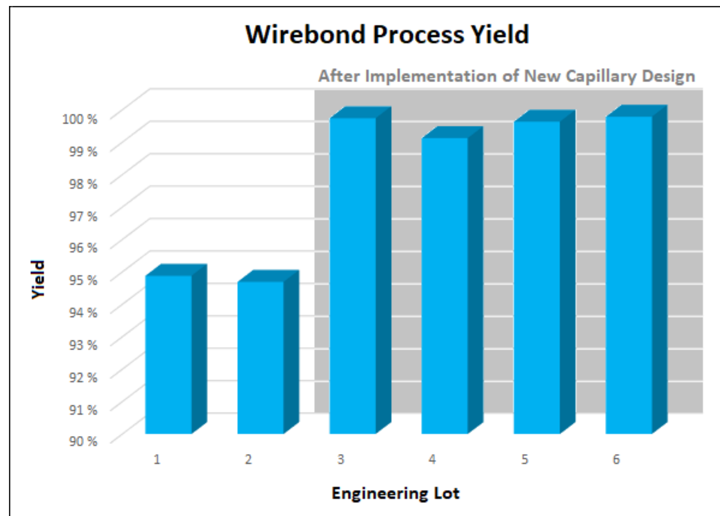

Fig. 3. Wirebond process yield performance

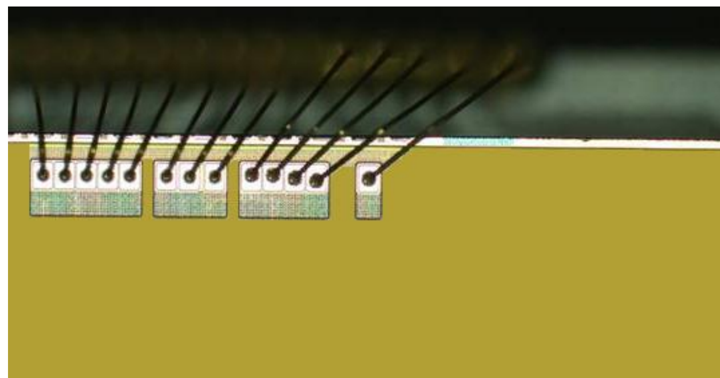

Fig. 4. Actual unit with improved wirebonding and no wire-to-wire shorting

the actual unit with no occurrence of wire-to-wire shorting defect.

3. CONCLUSION

With the wirebonding process optimization and redesigning a new capillary dimension, no wire-to-wire shorting defect and capillary hitting were observed on the succeeding engineering trials of the substrate LGA device. The development group was able to endorse a smooth process to the production group and no more concern on the test and finish performance in terms of the open-short (OS) test. For future works, the learnings experienced on this paper could be applied on other devices with similar condition. Moreover, studies, works, and learnings discussed in [9-14] are helpful to further improve the wirebonding process.

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COMPETING INTERESTS

Authors have declared that no competing interests exist.

REFERENCES

1. Liu Y, et al. Trends of power electronic packaging and modeling. 10th Electronics Packaging Technology Conference. Singapore; 2008.

2. Tan CE, et al. Challenges of ultimate ultra-fine pitch process with gold wire & copper wire in QFN packages. 36th International Electronics Manufacturing Technology Conference. Malaysia. 2014;1-5.
3. Saha S. Emerging business trends in the semiconductor industry. Proceedings of PICMET '13: Technology Management in the IT-Driven Services (PICMET). USA. 2013;2744-2748.
4. Yeap LL. Meeting the assembly challenges in new semiconductor packaging trend. 34th IEEE/CPMT International Electronic Manufacturing Technology Symposium (IEMT). Malaysia. 2010;1-5.
5. Harper C. Electronic packaging and interconnection handbook. 4th ed. McGraw-Hill Education, USA; 2004.
6. Greig W. Integrated circuit packaging, assembly and interconnections. 1st ed. Springer, USA; 2007.
7. Nenni D, McLellan P. Fabless: The transformation of the semiconductor industry. Create Space Independent Publishing Platform, USA; 2014.
8. May GS, Spanos CJ. Fundamentals of semiconductor manufacturing and process control. 1st ed., Wiley-IEEE Press, USA; 2006.
9. Moreno A, et al. Enhanced loop height optimization for complex configuration on QFN device. 2020 IEEE 22nd Electronics Packaging Technology Conference (EPTC). Singapore. 2020;182-184.
10. Gan C, et al. Wearout reliability and intermetallic compound diffusion kinetics of Au and PdCu wires used in nanoscale device packaging. Journal of Nanomaterials. 2013;1-9.
11. Ling J, et al. Wire bond reliability – An overview on the mechanism of formation/growth of intermetallics. Semicon. Singapore; 2008.
12. Pulido J, et al. Wirebond process improvement with enhanced stand-off bias wire clamp and top plate. Journal of Engineering Research and Reports. 2020;9(3):1-4.
13. Dresbach C, et al. Local hardening behavior of free air balls and heat affected zones of thermosonic wire bond interconnections. European Microelectronics and Packaging Conference. Italy. 2009;1-8.
14. Sumagpang A Jr., et al. Package design improvement for wire shorting resolution. Journal of Engineering Research and Reports. 2020;11(2):41-44.

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